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09/353,847	07/15/1999	HYUN CHANG LEE	8733/PD-6981	4171

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EXAMINER	
NGUYEN, JIMMY H	
ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/353,847	LEE ET AL.	
	Examiner	Art Unit	
	Jimmy H. Nguyen	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-11 and 19* is/are rejected.

7)☒ Claim(s) *7,12-18 and 20-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is made in response to applicant's Request For Reconsideration filed on 04/04/2005. Claims 1-26 are currently pending in the application. An action follows below:

Notice to Applicants

2. It is noted to Applicants that the original specification and drawing expressly disclose **a gate low voltage generator 4** (see Figs. 6 and 7) comprising **an electric charge accumulator 56** (may correspond to the claimed voltage enhancing device of claims 11-26) and **a low voltage selector 54**. See Figs. 7 and 9. However, claims 11-26 recite two separate elements, **a gate-off (or gate) voltage generator** and a voltage enhancing device. Examiner really confuses the claimed **gate-off (or gate) voltage generator** corresponding to either a gate low voltage generator 4 or a low voltage selector 54. Accordingly, the following drawing objection and claim objection are made.

3. It is suggested to Applicants to use the same references disclosed in the specification and drawing in order to avoid confusion and to clarify the claimed invention.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features, "a gate voltage generator" of claims 11, 12, 14, and 15, "a gate off voltage generator" of claims 19, 20, 22, and 23, and "a voltage enhancing device" of claims 11, 12, 15, 19, 20, and 23, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing

sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 10, 20, 22, and 23 are objected to under 37 CFR 1.75(a) because although these claims meet the requirement 112/2d, i.e., the metes and bounds are determinable, however, the following changes should be made:

Regarding to claim 10, "the step of raising a voltage" in lines 1-2 should be changed to -- the step of applying said higher level voltage--, so as to make the claimed feature consistent with the feature of independent claim 9.

Regarding to claims 20, 22 and 23, "gate" in line 1 should be changed to -- gate-off-- or an appropriation, so as to make the claimed feature consistent with the feature of independent claim 19 in light of the specification.

It is in the best interest of the patent community that applicant, in his/her normal review and/or rewriting of the claims, to take into consideration these editorial situations and make changes as necessary.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 5, it is not clear what the applicant means "wherein the level shifting means includes allows a voltage level ... power-off", i.e., the level shifting means must includes an element rather than an act of allows a voltage level.

It is noted applicants that due to the above 112 rejection to claim 19, the following art rejections to claim 5 are based as best understood by the examiner.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-5, 9-11, and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakaedani et al. (US 6,064,360), hereinafter Sakaedani.

As per claims above, the claimed invention reads on the Sakaedani reference as follows: Sakaedani discloses a liquid crystal display (LCD) device (see Fig. 3 and col. 3, lines 57-58) and an associate method for eliminating a residual image on the LCD device (see Fig. 3) comprising gate lines (32) and data lines (source lines or data lines, see col. 3, line 63, also best seen in Fig. 1) intersectingly arranged to form liquid crystal cells, each liquid crystal cell having a thin film transistor (31a) (see Fig. 3); a gate driver (a gate line driver circuit 33, Fig. 3) connected to the gate lines to enable thin film transistors (31a) connected to the gate lines; a gate-on voltage generator (a portion of a voltage generator circuit 34 that produces a gate-on voltage Vgh to enable thin film transistors 31a, see Fig. 3, col. 4, lines 1-5, and col. 3, lines 63-66); and a gate-off voltage generator (level shifting means of claim 1 or a device of claim 11) (a generator comprises a portion of a voltage generator circuit 34 that produces a voltage Vgl and element 35, see Fig. 3). Sakaedani also teaches the gate-off voltage generator comprising a voltage enhancing device (a charge storage circuit 36, see Fig. 3) including means for charging electric charges upon power-on of the LCD (see col. 4, lines 14-22) and voltage selecting means (a circuit comprises a portion of a voltage generator circuit 34 that produces a voltage Vgl and elements 37-39, see Fig. 3) for allowing a voltage charged in the charging means (36) to be applied to the gate lines upon power-off of the liquid crystal display panel (see col. 4, line 50 through col. 5, line 20). Sakaedani also teaches the voltage enhancing device (36) including a capacitor (C1) (see Fig. 3). Sakaedani teaches the gate-off voltage generator including a P-channel transistor (40), connected between a first voltage source (Vdd) and a second voltage source (GND), and

receiving the first voltage source (Vdd) and a second voltage source (GND) to generate a gate-off voltage (Vgl) having a first voltage level (e.g., -10V) for turning off the TFT (31a) to the gate line upon power-on (see col. 3, line 66 through col. 4, line 5) and a second voltage level (e.g., about +2V) higher than the ground voltage (0V) to the gate lines upon power-off (see col. 4, line 50 through col. 5, line 15). Sakaedani also teaches the charge storage circuit for accumulating electric charges during power-on and discharging the accumulated electric charges into the gate line during power-off (see col. 4, line 14 through col. 5, line 15). Accordingly, the elements and the steps in the claims above are read in the reference.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-6, 8-11 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art hereinafter AAPA, and further in view of Sakaedani.

As per claims 1, 11 and 19, the claimed invention reads on AAPA as follows: AAPA discloses a liquid crystal display (LCD) device (see Fig. 1 and page 2, line 12) comprising gate lines (11) and data lines (13) intersectingly arranged to form liquid crystal cells (12), each liquid crystal cell having a thin film transistor (10); an inherent gate driver connected to the gate lines (11) to enable TFTs (10) connected to the gate lines; an inherent gate-on voltage generator for producing a voltage higher than a threshold voltage to enable TFTs (10) (see page 2, lines 20-22); and a gate-off voltage generator (or level shifting means of claim 1 or a device for

eliminating residual image of claim 11), which is shown in Fig. 3, receiving a power supply (Vdd) and a ground voltage (see Fig. 3), including a transistor Q1 connected between the voltage Vdd and GND and providing a first voltage level for turning off the TFTs 10 to the gate lines upon power-on (see page 2, lines 28-30, "When ... a voltage level less than the gate threshold voltage Vth is supplied to gate lines 11 ..."). Accordingly, AAPA discloses all the claimed limitations of claims 1, 11 and 19 except for the feature, "the level shifting means applying a higher voltage level than the ground voltage to the gate lines upon power-off" of claim 1, or "a voltage enhancing device" of claims 11 and 19.

However, Sakaedani discloses a related LCD device comprising a gate-off voltage generator (or level shifting means) comprising a voltage enhancing device (a charge storage circuit 36, see Fig. 3) including including a capacitor (C1) (see Fig. 3) coupled to the output (Vgl) and the second voltage source (GND), wherein when the first voltage source (Vdd) is turned on, the capacitor is charged and when the first voltage source (Vdd) is turned off the capacitor (C1) boosts the gate off voltage (Vgl) to a level of +2V at the output to be higher than a threshold voltage of the thin film transistor (31a) (see col. 4, line 14 through col. 5, line 15). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide the voltage enhancing device of Sakaedani in the gate-off voltage generator (or level shift means) of AAPA, as taught by Sakaedani, because this would effectively remove the afterimage display after the turn-off of the power, which is due to the load capacitance in the TFT type LCD, as taught by Sakaedani (see col. 2, lines 29-32).

As per claims 2 and 3, AAPA discloses the first voltage level having a lower voltage level than a minimum value of the image signals and being a voltage applied to the gate lines when the liquid crystal display panel is in operation (see page 2, lines 28-31).

As per claim 4, Sakaedani teaches the voltage enhancing device (36) including means for charging electric charges upon power-on of the liquid crystal display panel and voltage selecting means (a circuit including elements 37-39) for allowing a voltage charged in the charging means to be applied to the gate lines upon power-off of the liquid crystal display panel. See col. 4, line 14 through col. 5, line 15.

As per claim 5, Sakaedani teaches the voltage enhancing device providing a voltage level of +2V at the gate line during the power-off (see col. 4, line 50 through col. 5, line 15).

As per claim 6, AAPA discloses the level shifting means including a zener diode (ZD) for applying a negative input voltage (VEE) lowered by its breakdown voltage to each one of the gate lines, and a transistor (Q1) connected between the each one of the gate lines and the ground voltage to switch a current path to bypass a voltage at the gate line to the ground voltage during power-off. Sakaedani teaches the voltage enhancing device including a capacitor (C1) for charging electric charge with an input charge voltage (Vdd) until a time of power-off and for applying a voltage (+2V) higher than the ground voltage to the each one of the gate lines upon power-off.

As per claim 8, AAPA discloses the level shifting means further including an alternating current voltage source (Ac) (see Fig. 3) for supplying an alternating current voltage to the gate lines, and a coupling capacitor (Cc) for eliminating a direct current component included in the alternating current voltage (see Fig. 3).

As per claims 9 and 10, these claims are similar to claim 1 above except they are method claims. Accordingly, these claims are rejected for the same reason set forth in claim 1 above.

Allowable Subject Matter

12. Claims 7, 12-18, and 20-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if overcome the claim objection above (to claims 20, 22, and 23).

13. The following is a statement of reasons for the indication of allowable subject matter: the claimed invention is directed to a device for eliminating residual image on a LCD device. Dependent claim 7 identifies the uniquely distinct features, "wherein the level shifting means further includes: a first resistor ...; and a second resistor ... power-off". Dependent claims 12 and 20 identify the uniquely distinct features, "the voltage enhancing device includes a resistor ... time constant" (see last 4 lines of these claims). Dependent claims 15 and 23 identify the uniquely distinct features, "wherein the gate voltage generator includes a resistor ..., and the voltage enhancing device includes a resistor ... source". The closest prior art, Sakaedani as discussed above, either singularly or in combination, fails to anticipate or render the above underlined limitations obvious.

Response to Arguments

14. Applicant's arguments, see page 7-8 of the amendment, filed 04/04/2005, with respect to the rejection(s) of claim(s) 1-26 under 35 USC 103(a) as being unpatentable over Moon et al. in view of Tsuchi et al., in the Office Action dated 12/03/2004 have been fully considered and are

persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Sakaedani above.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy H. Nguyen whose telephone number is 571-272-7675. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached at 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JHN
November 9, 2005

Jimmy H. Nguyen
Primary Examiner
Art Unit: 2673